PM1K

CogniMem Prototyping board

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COGNIMEM
technologies, inc.

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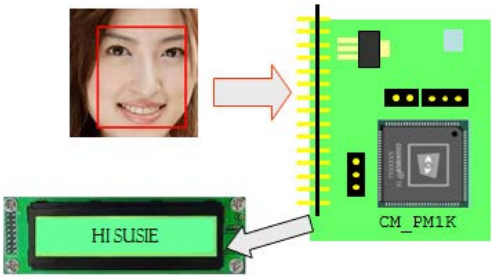
Table of Contents

Introduction

PM1K is a miniature PCB board with a convenient 30-pin connector interfacing to the I2C bus and digital input bus of the CogniMem CM1K chip.

CogniMem is a high-performance pattern recognition chip featuring a network of 1024 neurons operating in parallel. The recognition logic built into the CM1K chip allows broadcasting a video or digital signature directly to the input bus of the chip and read the response of the neuron with the best match in real-time.

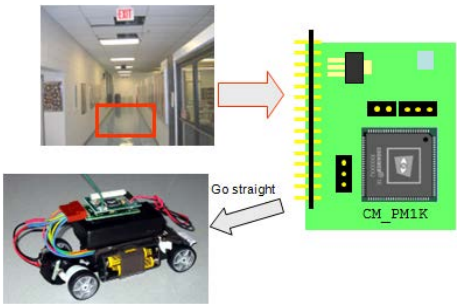


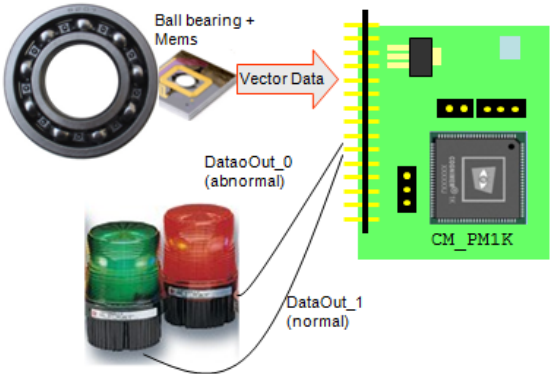
Example 1: Door control

Connect a video CMOS sensor to the PM1K digital input bus. Connect a PIC controller or else to the I2C lines and send commands to learn a specific person present in the field of view and launch the continuous recognition. Read the response over the I2C lines and display the name of the person on an LCD.

Example 2: Motion control

Connect a video CMOS sensor to the PM1K digital input bus and a controller to the I2C lines. Send I2C commands via push buttons to teach if the robot shall turn left or right to keep in the middle of the hallway. Launch the continuous recognition and connect directly the output lines of the PM1K to a servo controller in order to rotate the sensor.





Example 3: Detection of abnormal vibrations

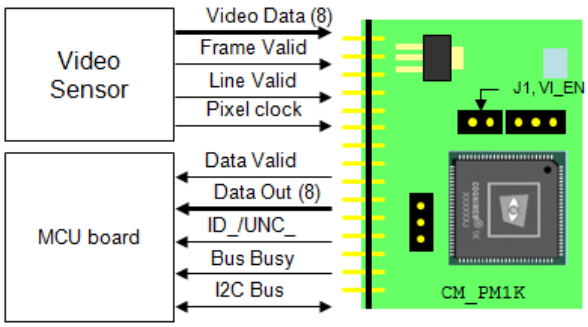
Connect a MEMS to the PM1K digital input bus and a controller to the I2C lines. Send I2C commands via push buttons to teach when the vibration is normal. Launch the continuous recognition and connect directly the output lines of the PM1K to turn on a red LED in case the input signal is not recognized.

PM1K for Video Recognition

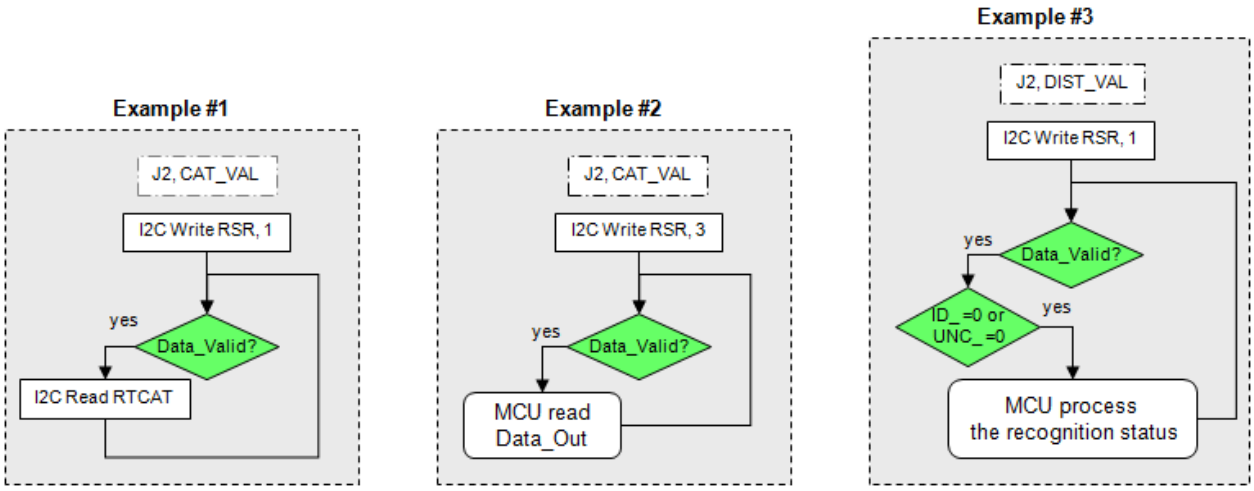
The CM_PM1K board is configured for video recognition by putting a jumper between pin 1 and 2 of J1. This enables the regional video feature extraction programmed in the CM1K chip.

Wire the output of your video sensor to the 30-pin header of CM_PM1K:

V CLK	Pixel clock (up to 27 Mhz)
V_FV	Frame Valid (high during a frame)
V_LV	Line Valid (high during a line)
V_DATA[7:0]	8 highest bits of the video data



The next diagrams illustrate different options to recognize an object in your video images. First, the real-time recognition logic is enabled by settings bit 0 of the RSR register to 1. The recognition starts immediately at the next Frame Valid pulse and applies to the default region of interest defined in the CM1K. This region occupies 1/3 of the video frame and is centered in the video frame.



- **Example #1** uses the I2C communication to retrieve the recognized category from the 16-bit RTCAT register of the CM1K chip.

- **Example #2** is suitable when the recognized categories range between 0 and 255. Bit 1 of the RSR is set to 1 to enable the output of the 8 lowest bits of the category to the Data_Out lines. The external processor can read this data when the DATA_VALID line pulses. This line is assigned to the CAT_VAL line of the CM1K through the Jumper J2.

- **Example #3** reads the status of the recognition (as opposed to the recognized category). It is suitable for an application which simply needs to verify that the region is recognized without uncertainty. This status is the NAND of the ID_ and UNC_ lines which can be read when the

DATA_VALID line pulses. In this case, DATA_VALID can be assigned to the DIST_VAL line of the CM1K which occurs 18 clock cycles before the CAT_VAL pulse.

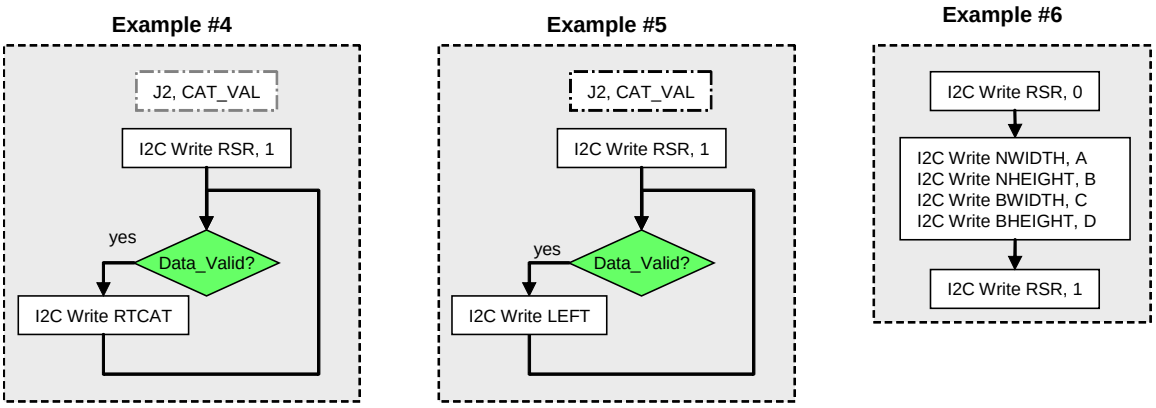
Unless the neurons have been loaded in advance with a knowledge through a series of I2C Write commands, the recognized category is 0x00 and the lines ID_ and UNC_ are both high.

- **Example #4**: The neurons are taught in real-time what to recognize by writing the CM_CAT register immediately after the fall of the CAT_VAL pulse following the frame where the example is seen.

- **Example #5**: The position of the region to learn or recognize is moved along the horizontal axis by writing the CM_LEFT register of the CM1K chip immediately after the fall of the CAT_VAL pulse and before the next Frame Valid.

All these commands can be sent when the B_BSY signal is low, but when the recognition logic is running, they must be completed before the next Frame Valid. Failure to do so can result in an improper feature extraction and therefore recognition or learning operation. When a sequence of commands must be executed (for example, to change the size of the region of interest), it is recommended to stop the recognition logic temporarily.

- **Example #6**: Changing the region of interest takes four Write commands. Stopping and re-starting the recognition logic is recommended.

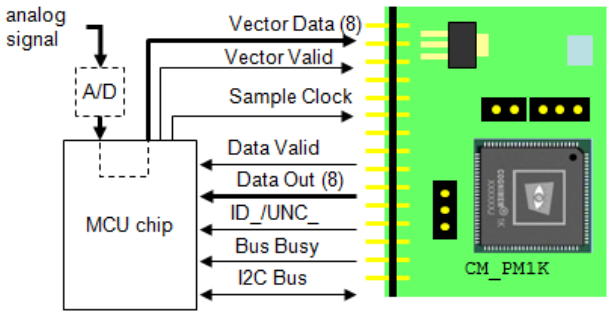


PM1K for Signal Recognition

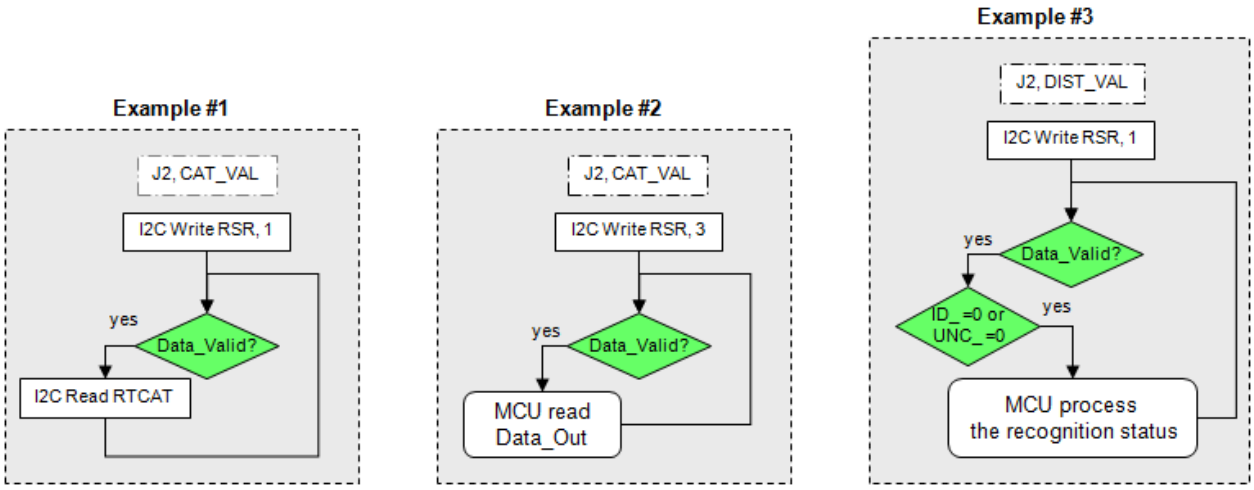
The CM_PM1K board is configured for signal recognition by removing the jumper J1.

Wire your signal digitized by the micro-controller through an A/D converter to the 30-pin header of CM_PM1K:

V CLK	Sample clock (<=27 Mhz)
V_DATA[7:0]	8 bits of the vector data
V_FV	Vector Valid (high during data input. The fall of this signal triggers the recognition of the vector.



The next diagrams illustrate different options to obtain the classification of the Vector Data. First, the real-time recognition logic is enabled by settings bit 0 of the RSR register to 1. The recognition starts immediately at the next Vector Valid pulse.



- **Example #1** uses the I2C communication to retrieve the recognized category from the 16-bit RTCAT register of the CM1K chip.

- **Example #2** is suitable when the recognized categories range between 0 and 255. Bit 1 of the RSR is set to 1 to enable the output of the 8 lowest bits of the category to the Data_Out lines. The external processor can read this data when the DATA_VALID line pulses. This line is assigned to the CAT_VAL line of the CM1K through the Jumper J2.

- **Example #3** reads the status of the recognition (as opposed to the recognized category). It is suitable for an application which simply needs to verify that the vector is recognized without uncertainty. This status is the NAND of the ID_ and UNC_ lines which can be read when the DATA_VALID line pulses. In this case, DATA_VALID can be assigned to the DIST_VAL line of the CM1K which occurs 18 clock cycles before the CAT_VAL pulse.

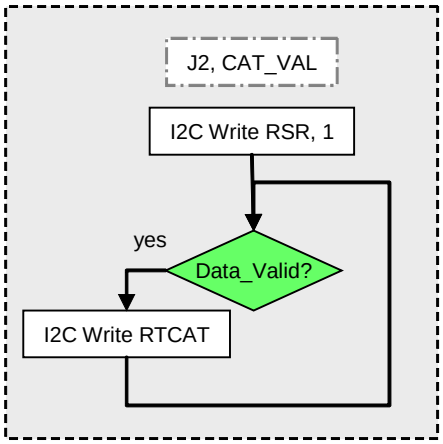
Unless the neurons have been loaded in advance with a knowledge through a series of I2C Write commands, the recognized category is 0x00 and the lines ID_ and UNC_ are both high.

- **Example #4**: The neurons are taught in real-time what to recognize by writing the CM_CAT register immediately after the fall of the CAT_VAL pulse following the frame where the example is seen.

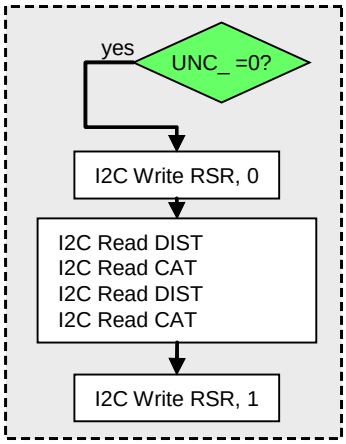
Other commands can be sent to the CM1K when the B_BSY signal is low, but when the recognition logic is running, they must be completed before the next Vector Valid. Failure to do so can result in an improper recognition or learning operation. When a sequence of multiple commands must be executed, it is recommended to stop the recognition logic temporarily.

- **Example #5**: A application might need to review cases of uncertainty in details by reading the distance and category registers of at least the first two top firing neurons. This requires at least four Read commands executed during a temporary interruption of the real-time recognition.

Example #4



Example #5



The I2C serial communication

The CogniMem CM1K chip is very easy to configure and control through two dozens registers which can be read and written via the I2C protocol described below.

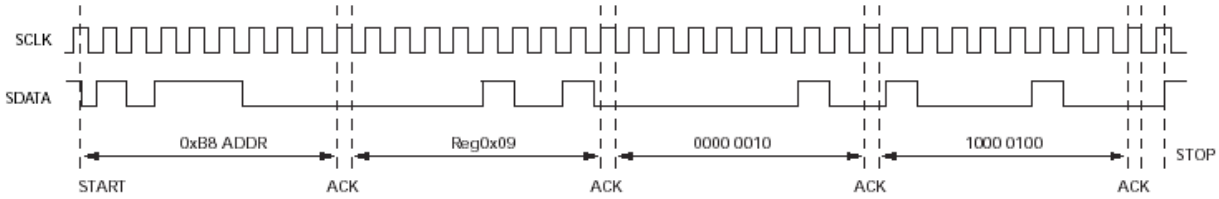
The I2C slave controller of the CM1K operates at a speed of 100 or 400 Kbits per second and converts the clock and serial data received on the I2C_SCK and I2C_SDA pins into an internal data strobe, Read/Write signal, register value and data value.

For a list of the CogniMem CM1K registers, please refer to the CM1K manual and to the CogniMem Technology Reference Guide.

Write sequence

A start bit given by the master, followed by the write Slave Address, starts the sequence. If the Address is 0x94, the CogniMem slave returns an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each data byte the slave gives an acknowledge bit. All 16 bits must be written before the register is updated. The master stops the writing sequence by sending a stop bit.

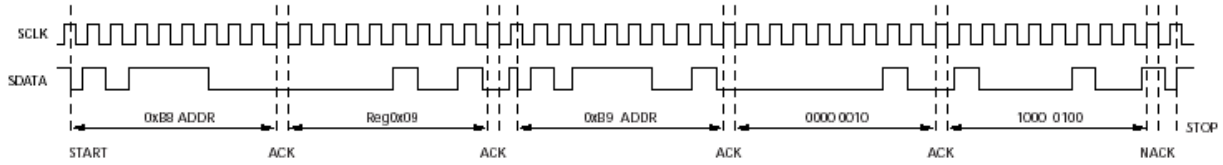
I2C Write sequence Write Slave Address + bit[0]=0 for Write (0xB8 in example below)
Write 8-bit Register value (0x09 in example below)
Write 16-bit Data value (0x0284 in example below)



Read sequence

A start bit given by the master, followed by the write Slave Address, starts the sequence. If the Address is 0x94, the CogniMem slave returns an acknowledge bit and expects the register address to come first. Then a start bit and the read address specifies that a read of the register is about to happen. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each eight-bit transfer. The data transfer is stopped when the master sends a no-acknowledge bit.

I2C Read sequence Write Slave Address + bit[0]=0 for Write (0xB8 in example below)
Write 8-bit Register value (0x09 in example below)
Write Slave Address + bit[0]=1 for Read (0xB9 in example below)
Read 16-bit Data value (0x0284 in example below)



Clock Timing constraints

To ensure the proper execution of a read command, the high period of the I2C-SCK signal must be greater than the time requested to retrieve the data value. The table below illustrates this arithmetic using the longest command executed by CM1K which takes 18 clock cycles (i.e. Read CAT register).

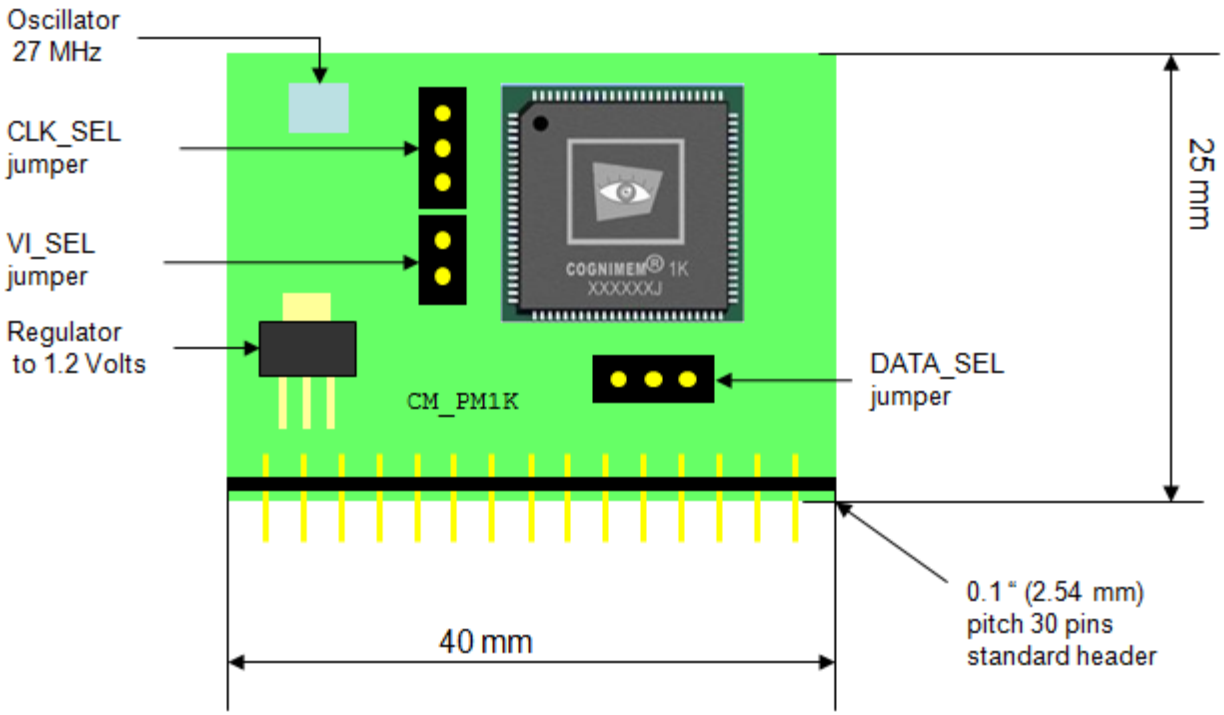
I2C master	I2C-SCK ½ period (us)	18 cc (ns)	Min G_clk (Mhz)
100 Kbit	5.00	277	3.6
400 Kbit	1.25	70	14.4

Execution Timing constraints

The I2C slave controller can start executing a command when the B_BSY signal is low.

When the recognition engine is running, this time frame can be quite short since B_BSY is high periodically. The registers RTDIST and RTCAT are latched after each recognition and can be read at any time by the I2C slave. However, any other command must be submitted carefully, that is after the rise of the CAT_VAL signal and terminated before B_BSY rises again.

Connectors and Jumpers



Jumpers

J1, VI_SEL

Video Select indicates if the digital input bus of the CM1K receives a video signal or a digital vector data. In the first case, the recognition engine of the CM1K is in charge of generating a vector from the video data prior to broadcasting it to the neurons. In the second case, the vector data is sent directly to the neurons. By default, there is no jumper between pins 1 and 2 to set the Video Enable.

J2, DATA_SEL

Data_Select indicates if the DATA_VALID output of the board shall be assigned to the DIST_VAL or CAT_VAL line of the CM1K chip. By default, the jumper is installed between pins 2 and 3 to assign CAT_VAL.

CAT_VAL and DIST_VAL are consecutive strobes which rise 18 clock cycles apart when a new vector is recognized by the real-time recognition logic. These lines are active when bit 0 of the RSR register is set to 1. The selection of DIST_VAL can be of interest to an application which only requires to know if an object is recognized or not (such as target tracking and anomaly detection). In this case, the status lines ID_ and UNC_ can be read when DIST_VAL pulses (i.e. 18 clock cycles before CAT_VAL).

J3, CLK_SEL

Clock_Select indicates if the operating clock shall come from the 27 Mhz oscillator of the board or an external clock. By default, the jumper is installed between pins 2 and 3 to use the internal clock.

Connector pinout

Power supply 3.3V
Power consumption .....approx 240 mA at 1.2V / 27 Mhz

Pin#	Abbrev	Signal	Pin#	Abbrev	Signal
1	GND	GND	2	VCC	VCC is 3.3 volts
3	DATA_VAL	Data Valid strobe	4	DATAO7	Output data 7
5	DATAO6	Output data 6	6	DATAO5	Output data 5
7	DATAO4	Output data 4	8	DATAO3	Output data 3
9	DATAO2	Output data 2	10	DATAO1	Output data 1
11	DATAO0	Output data 0	12	B_BUSY	Bus Busy
13	ID_	Identified status line	14	UNC_	Uncertain status line
15	V_CLK	Video/Vector clock	16	V_FV	Video Frame/Vector Valid
17	V_LV	Video Line Valid	18	V_DATA7	Video/vector data 7
19	V_DATA6	Video/vector data 6	20	V_DATA5	Video/vector data 5
21	V_DATA4	Video/vector data 4	22	V_DATA3	Video/vector data 3
23	V_DATA2	Video/vector data 2	24	V_DATA1	Video/vector data 1
25	V_DATA0	Video/vector data 0	26	I2C SDA	I2C data line
27	I2C SCK	I2C clock line	28	STANDBY	Standby (low power)
29	RESET_	Reset (low)	30	G_CLK	External clock

Input lines

RESET_

Global reset. Must be pulled down for a minimum of 5 clock cycles to reset the chip properly. The contents of all the neurons is cleared and all registers are set to their default values.

G_CLK

Operating clock. Depending on the CLK_SEL jumper settings, this clock can derive from the 27 Mhz oscillator of the board or from an external clock such as the sensor clock or else (up to 27 Mhz).

STANDBY_

This signal sets the chip in low-power mode by shutting down the G_Clock signal and putting the neurons in idle mode. It must be pulled down when the neurons need to be accessed which is whenever a Read or Write command is sent and when the recognition logic is running (between the fall of V_FV and the rise of CAT_VAL).

V CLK

Video Clock or Vector Clock depending on the VI_SEL jumper settings:

- If VI_SEL=1, V_CLK shall be the video clock signal of the sensor (up to 27 Mhz).
- If VI_SEL=0, V_CLK shall be the sampling clock of the V_DATA digital input. It does not have to be a periodic signal.

V_FV

Video Frame Valid or Vector Feature Valid depending on the VI_SEL jumper settings:

- If VI_SEL=1, V-FV stands for Frame valid and is a synchronization signal supplied by the video sensor. It must be high for the duration of the frame.
- If VI_SEL=0, V-FV stands for Feature Valid. It must be set high for the duration of the vector data transmission to the V_DATA bus. V_FV can be high for up to 256 pulses of V_CLK and must stay low afterwards at the minimum until the CAT_VAL line pulses. V_FV must be changed at the negative edge of V_CLK.

V_LV

Video Line Valid signal of the sensor (used only if VI_SEL=1). It must be high for the duration of a line of pixels.

V_DATA

Video Data or Vector Data depending on the VI_SEL jumper settings:

- If VI_SEL=1, this 8-bit data signal must be connected to the 8 highest bit of the video signal.
- If VI_SEL=0, this 8-bit data signal can come from a sensor or be generated by an external controller.

Output lines

B_BSY

The Bus Busy line is high during the execution of an internal cycle such as a reset cycle, a recognition cycle, the execution of an I2C read or write command received from an external controller, etc. An external master controller must verify that B_BSY is low prior to sending a command. Otherwise the command will be discarded. This signal is updated at the negative edge of the G_CLK.

DATA_VAL

DATA_VAL stands for Data Valid and is assigned to the DIST_VAL or CAT_VAL pulse of the CM1K chip depending on the DATA_SEL jumper settings. In either case, the pulse only occurs if the real-time recognition logic is running (i.e. RSR[0]=1).

- The Distance Valid signal rises on the negative edge of G_CLK when the real time distance register (RTDIST) read during the last recognition is available on the DATA output bus. This strobe lasts one clock cycle.
- The Category Valid signal rises on the negative edge of G_CLK when the real-time category register (RTCAT) read during the last recognition is available on the DATA output bus. This strobe lasts one clock cycle.

DATAO[7:0]

The DATAO lines are assigned to the 8 lowest bit of the real-time category register. This value is updated when the CAT_VAL line of the CM1K pulses and under the condition that its output is enabled (i.e. RSR[1]=1).

ID_

The Identified line is pulled down when the neurons recognizing the last vector are all in agreement and return the same category. This line is updated each time the last component of a vector is broadcasted to the neurons by writing the LCOMP register through the I2C bus or through the real-time recognition logic of the CM1K.

UNC_

The Uncertain line is pulled down when the neurons recognizing the last vector are NOT all in agreement and do not return the same categories. This line is updated each time the last component of a vector is broadcasted to the neurons by writing the LCOMP register through the I2C bus or through the real-time recognition logic of the CM1K.

PM1K Schematics