COGNIMEM™ TECHNOLOGY OVERVIEW

TECHNICAL BRIEF

The CogniMem Technology is a pattern recognition accelerator which enables practical usage of neural network and KNN algorithms for markets ranging from smart sensing to high performance computing.

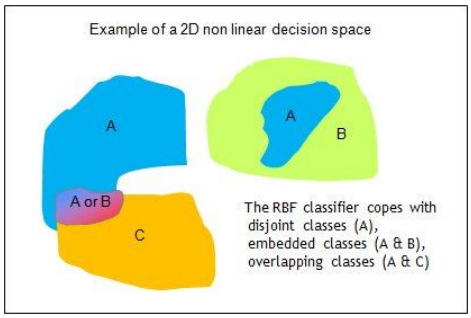
A CogniMem network is a chain of identical cells (i.e. neurons) addressed in parallel with their own "genetic" material to store, learn and recall patterns without running a single line of code and then reports to a supervising unit. The neurons collaborate with each other through a bi-directional parallel bus which is the key to accuracy, speed of recognition, real-time learning, and adaptation.

CogniMem can be considered as one of the following three components:

- A real-time trainable neural network
- A KNN engine with results in microseconds
- A low-power pattern recognition chip for embedded devices as well as high-performance computing systems.

Real-Time Trainable Neural Network

The CogniMem neural network is a Radial Basis Function (RBF) classifier with built-in model generator. This classifier is used with a high degree of interest in research communities for non-linear mapping and classification, function approximation and data clustering. The CogniMem RBF network is highly adaptive and capable of real-time reinforced learning. Its architecture enables the tracing of examples which bring novelty and commit new neurons.



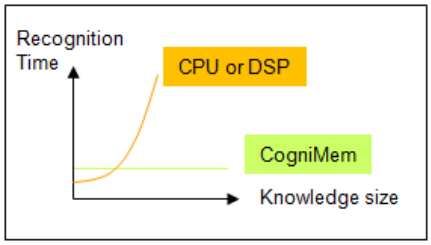
Recognition time is independent of the number of models retained by the neurons so you can teach all the examples you choose to teach and do not need to find compromises and work-arounds to obtain practical response time.

KNN in Microseconds

K Nearest Neighbor is an algorithm that is very simple and works incredibly well for the closest match and pattern classification.

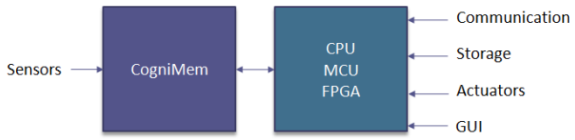
The clever use of KNN can make things very simple for applications ranging from vision to protein identification to computational geometry to data mining and so on. The downside of the algorithm is that it is highly computational, but thanks to the CogniMem parallel architecture, its execution time

becomes independent of the number of trained examples and solely proportional to the number of input vectors, their length and the value K.

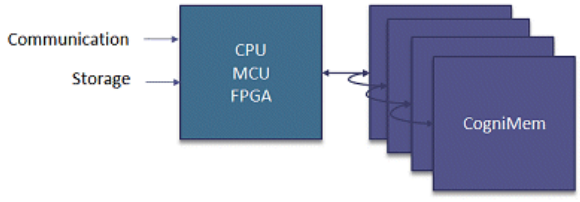


Pattern Recognition Chip for Embedded & High-Performance Computing

The CogniMem chip can be used as a companion chip to sensors enabling real-time data recognition and transmission only when the information is of interest.



Beyond the arena of the low-cost, low-power embedded systems, multiple CogniMem chips can be daisy-chained to build massively parallel data mining systems with unlimited capacity and a recognition time independent of the size of the knowledge base.



Building banks of CogniMem chips is effortless. On the hardware side, it simply requires daisy-chaining the chips and connecting them together through their parallel bus. On the firmware side there is no impact whether your hardware uses a single chip or a bank of many chips. The chain of chips is seen and accessed as a single network.

Background and Implementations

The concept of CogniMem was invented in 1993 by Guy Paillet, one of the founders of CogniMem Technologies Inc., and implemented in a collaborative effort with IBM into an ASIC trademarked by IBM as the Zero Instruction Set Computer (ZISC) chip.

It is the merger of two concepts: (1) A non-linear classifier called Restricted Coulomb Energy, invented in 1982 by Nobel Prize Winner Leon Cooper, et al, which was derived from Bruce Batchelor's work and, (2) a hardwired parallel architecture designed for the CERN's UA1 experiment in 1984 lead by Nobel Prize winner Carlo Rubia.

Two generations of ZISC were released: ZISC36 with 36 neurons in 1993 and ZISC78 with 78 neurons in 1999. Unfortunately, IBM discontinued the manufacturing of the ZISC chip in 2001. In 2007, Guy Paillet and Anne Menendez (also a founder of CogniMem Technologies, Inc.) started the design of a replacement for the ZISC. The goal was to fit one thousand (1K) neurons on each chip and add features to the architecture. OKI was contracted to manufacture the ASIC and the first batch of CM1K chips was produced in January 2008.