CogniMem Technology

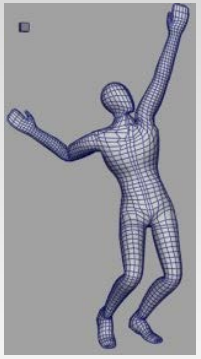
A unique technology
making pattern recognition
affordable, practical and ubiquitous

Pattern Recognition is everywhere…

Blood to data

Image Analytics

3D rendering



Video Analytics

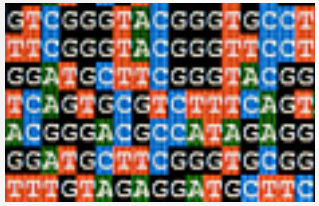
Data Storage/
Compression/
De-Duplication

Data Transmission
Packet filtering

Sound/Vibration

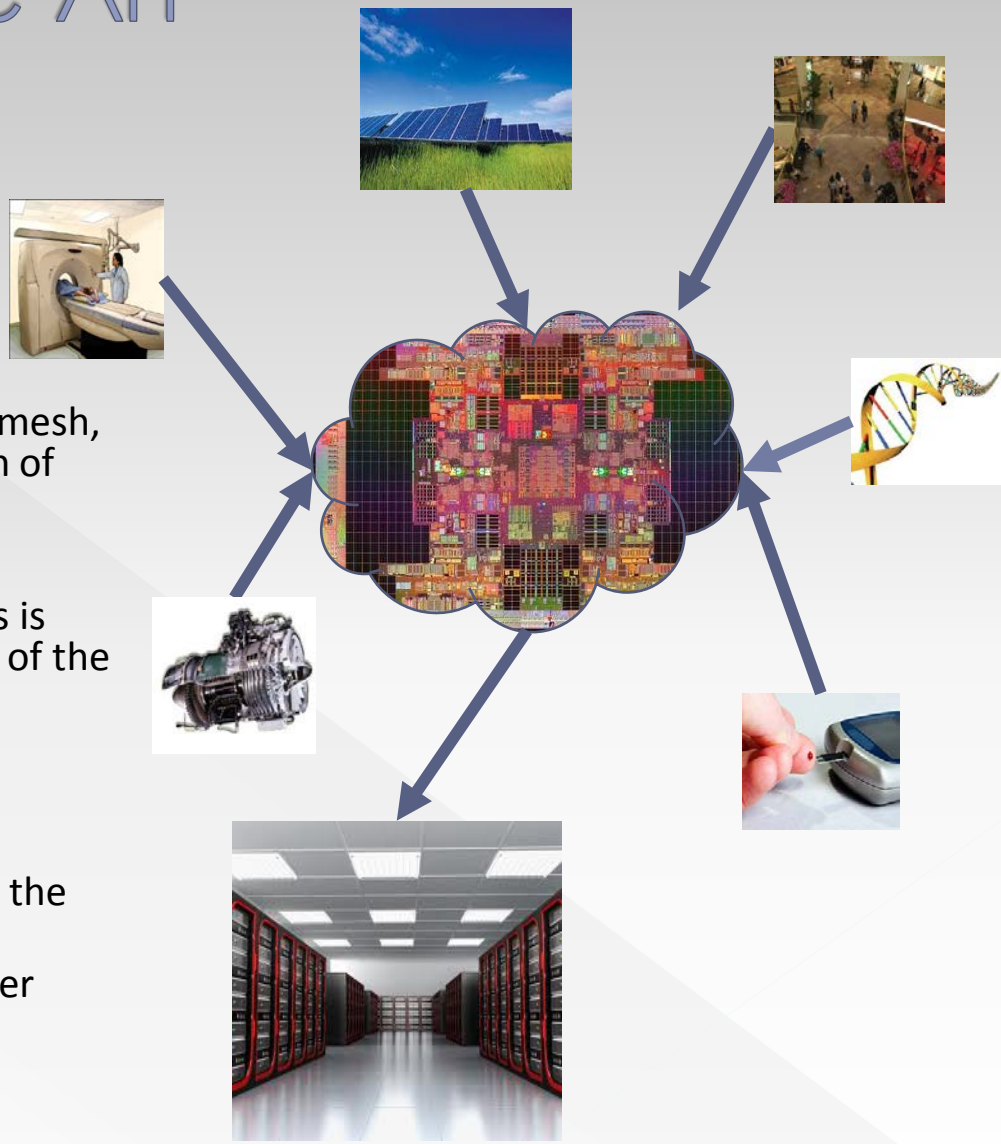
EKG/EEG

Bioinformatics



The State of the Art

- Multi-core processors
  - On going research for topologies interconnecting cores (bus, ring, 2D mesh, and crossbar) and the parallelization of software
- Server farms
  - The performance of the server farms is typically limited by the performance of the data center's cooling systems and electricity cost rather than by the performance of the processors“
- The Internet of the Things (IBM)
  - Claimed intelligence often limited to the ability to transmit
  - Decision is not yet built into consumer appliances

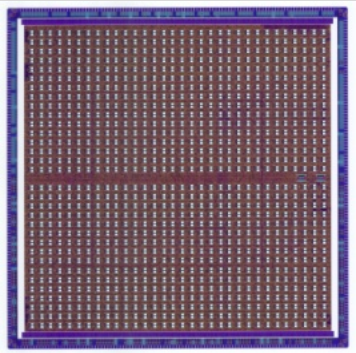


The CogniMem offering:

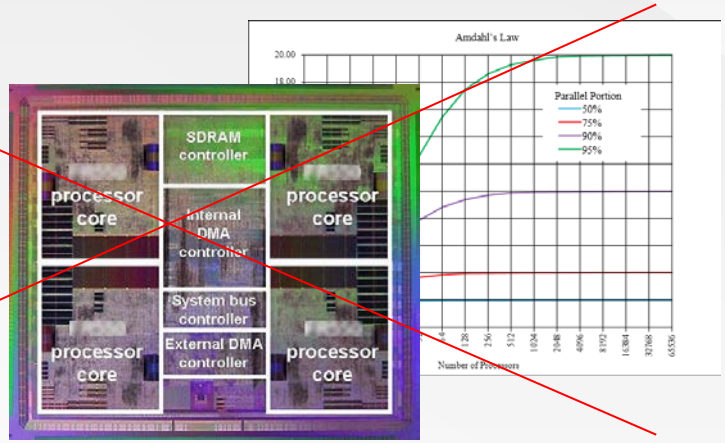
- Memory and processing logic combined in a same element
- Natively parallel architecture of identical elements
- Simple access control independent of the number of elements connected in parallel

- Eliminate dependency from Amdahl's law
- Eliminate the memory misery bottleneck
- Reduce power consumption

CM1K = 1024 identical cognitive memories in parallel
<27 Mhz, <0.5 W



A multicore processor surrounded by DMA and SDRAM controllers
> 1 Ghz, >10 W



How does CogniMem compare to other memories?

Where did I park my car?

Standard Memory way:

Walk from car to car until you find yours

(sequential search can take minutes!)

Cognitive Memory way:

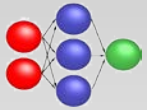
Click your electronic control and wait for your car to respond

(Reactive search takes microseconds)

The origins of CogniMem

The merger of two concepts

Non-linear classifier



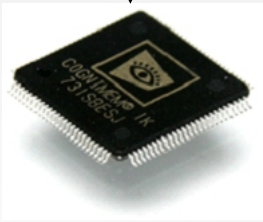
1982 - Restricted Coulomb Energy invented by Nobel prize Winner Leon Cooper and All, derived from Bruce Batchelor's work

Hardwired parallel architecture

1984 - CERN's UA1 experiment lead by Nobel prize winner Carlo Rubbia

1993 - ZISC (Zero Instruction Set Computer) designed by IBM France and Guy Paillet featuring 36 and later 78 neurons

2 in 1 chip:
- Parallel reactive memories,
- High speed pattern recognition chip



2009 - CM1K (Cognitive Memory) designed by Anne Menendez and Guy Paillet featuring 1024 neurons

Technological advantages

- Content adressable memories
  - Exact or fuzzy pattern matching
- Massively and natively parallel
- Scalable knowledge base
- Constant recognition in microseconds
- Low power consumption
- Automatic model generator
- Simple set of 15 R/W registers

The CogniMem applications

- *Cognitive Sensing*
  - *Integrate low-power pattern recognition into sensors, enabling near line "cloud computing"*
  - *Enable sensors to decide and take action (actuation or transmission)*
- *Cognitive Computing*
  - *Highly scalable, truly parallel and low-power solution for data mining*
  - *Sensor fusion, Contextual understanding, hypothesis generation*
- *Cognitive Networking*
  - *High speed pattern matching in data streams*
  - *High speed novelty or anomaly detection in data streams*

Market Potential

- Functional groups
  - Discrete visual objects, surface
  - Target, gesture, video analytics, smart motion
  - Sound, voice
  - Signal (accelerometer, EEG, EKG)
  - Data packets, IPV6, statistics, measurements
- Market groups
  - Factory automation (industry, display and semi-conductor)
  - Automotive and Transportation
  - Health Sciences
  - Defense and Security
  - Consumer electronics
  - Energy and power
  - Communication