November 11, 2011

Volume 1, Issue 1

COGNIMEM Technologies, Inc.

A Novel Approach to Modern Computing…

THE COGNIMEM COMMUNIQUE`

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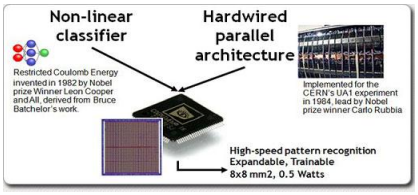
CTI's involvement at IJCNN-2011

CogniMem was one of the proud sponsors at the 2011 International Joint Conference on Neural Networks (IJCNN-2011) held in San Jose, CA. during the week of July 24, 2011.

There were many Plenary Speakers at the conference but of note is one who reinstated the potential of Neural Networks in cognitive computing– Mr. Dharmendra Modha. Mr. Modha is working on the DARPA cognitive computing project syNAPSE; for IBM at their IBM Almaden Research Center.

This project consists of making a chip that can emulate a human's brain. At this conference, syNAPSE's representative disclosed that the first phase of the process has been completed, and work has already begun on phase 2.

In 1993, Guy Paillet, one of the founders of CogniMem™ Technologies Inc, presented the concept of a self organizing, trainable parallel neural network chip to IBM and worked with a team at the IBM lab in Essonnes, France lead by Pascal Tanhoff. The outcome of this collaborative effort was an ASIC trademarked by IBM as the Zero Instruction Set Computer (ZISC) chip. Two generations of ZISC were released: ZISC36 with 36 neurons and ZISC78 with 78 neurons. In 2008, Anne Menendez (one of the other founders of CogniMem™ Technologies Inc.) and Guy Paillet designed the CM1K. This was an advanced version of ZISC78 with 1k neurons along with some additional features.



Click to learn More

CogniMem™ Technologies Inc. is working on Big Artificial Brain (BAB), which will demonstrate a truly parallel computing system capable of recognizing a pattern of 256 bytes among 1 million neurons in 10 microseconds.

Numerous people stopped by our booth at IJCNN and expressed excitement at the availability of CogniMem's products. Now, no longer people have to depend upon Von Neumann platforms and very slow simulations!

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Developer's corner

"…contact us for your copy of this additional evaluation tool…"

The Penguin has neurons. Our V1KU evaluation system now supports the Linux platform with a Java based tool in addition to Windows platform with a Dot-net based tool.

If you have already purchased our V1KU evaluation system, contact us for a copy of this additional evaluation tool. Those new to CogniMem, both Dot-Net and Java based tools are delivered with our V1KU kit.

V1KU

Visit us at The Super Computing Conference in Seattle.

"Exhibit hall… will have exhibitors from all over the world representing diversity, future potential and applications on contemporary technologies along with supercomputing."

Supercomputing has been mankind's quest since the beginning of the technology era. Supercomputing is a very intriguing and complicated subject. SC11 will provide an international platform for all involved communities to exchange information on collaborations for research, innovating high performance computing applications, scientific discovery and scholarships.

This conference will also provide a chance to explore technical and community programs along with its Exhibit hall.

SC11's Exhibit hall will have exhibitors from all over the world representing diversity, future potential, and applications in contemporary technologies along with supercomputing.
CTI will also be actively participating at this event as an exhibitor and will highlight the "CogniBlox"

CogniBlox

Come see us in Seattle!
Booth Number: 4509, 6th Floor.
Washington State Convention center, Seattle, WA

Click for more information!

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Article- White paper

CogniMem, Paradigm shift in artificial intelligence

"…an essential difference between the biological approach and the computing approach of intelligence lays in the fact that biology uses active memory cells (neurons) while computers use a procedural activity involving the "fetch, decode and execute" model..."

It is well described in Jeff Hawkins' landmark book "On Intelligence" that an essential difference between the biological approach and the computing approach of intelligence lays in the fact that biology uses active memory cells (neurons) while computers use a procedural activity involving the "fetch, decode and execute" model. The computer model is similar to someone who would need to read both the car user's manual and the vehicle transportation civil code as he drives. Indeed everybody knows that this is not the way to drive! The fact that while initial attempts to drive and obtain a driver's license is a supervised (somewhat procedural) learning experience, surviving the early days of driving allows us to permanently "memorize" the way of operating the vehicle and behave (more or less) within the driving code. Up to now, no computer has the ability to discard the procedural operation.

The fact that computer architecture is based on the segregation of the programs and the data prevents any evolution in this direction. What we are introducing in this paper is a concept that we have matured over the past twenty years and which closely matches a solid-state semiconductor technology with biological models. We call it the CogniMem Technology (i.e. Cognitive Memory).

The CogniMem Technology is to human brain is what the plane of the Wright Brothers was to the bird or what the robot arm is to a human arm. CogniMem is inspired by years of thinking and enlightened discussions with persons such as Prof. Carlo Rubbia and Leon N. Cooper, both Nobel Laureates, and Prof. Bruce Batchelor, a great pioneer in pattern classification. The combination of 30 years of hardware experience and computer anthology, the opportunity to be the lead hardware designer of a huge parallel computing experience in 1984 for the UA1 experiment at CERN and to meet and work with Leon Cooper in 1988 and cooperate with him for 4 years at Nestor Inc. led Mr. Guy Paillet to think about the silicon implementation of neural cells working in parallel. Due to these previous developments, it was possible to convince the IBM Semiconductor Labs in Paris to design and manufacture the first issue of the CogniMem technology, the ZISC® chip (Zero Instruction Set Computer). The basic architectural concept was delivered to IBM in February 1993 and the first ZISC36 chip with 36 neurons was powered up successfully in October 1993. A new chip design never went so fast at IBM, thanks to its orthogonal simple architecture as simple as 36 connectable digital neurons.

Read more…

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