

The CM IP package enables a thorough evaluation of our IP blocks prior to their integration into an ASIC or SOC. It is composed of an evaluation board featuring an FPGA in which the selected IP cores can be instantiated as well as a connector to support the addition of a CMEnK neuron expansion module. The IP cores are delivered as black boxes and can be instantiated multiple times in the FPGA.

This product is subject to license for purchase in the United States. It is licensed to customer for evaluation purposes and internal use only. It cannot be sold by customer nor integrated into a commercial product.

Library of IP cores

Neuron cluster IP Core

Clusters of 16 neurons can be instantiated multiple times for intra-chip network expansion. Building a network of 32 neurons is as simple as instantiating two clusters of 16 neurons, wiring their parallel buses together and passing the daisy chain output line of one to the daisy chain input of the second one.

The neuron cluster IP core is a chain of 16 identical neurons operating in parallel. A neuron is an associative memory which can autonomously compare an incoming pattern with its reference pattern. During the recognition of an input vector, all the neurons communicate briefly with one another (for 16 clock cycles) to find which one has the best match. Refer to the CM1K datasheet for more information about the neurons' behavior and performance.

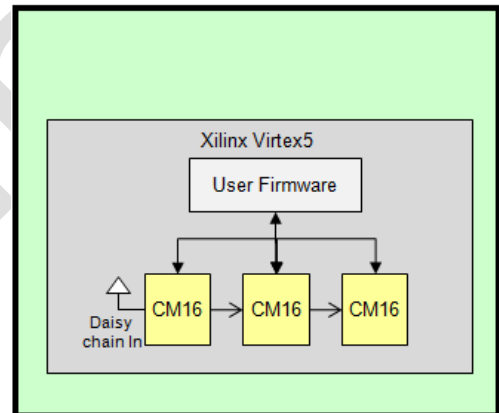
Optional generic recognition stage

This IP core allows sampling patterns received through a dedicated input bus to be submitted automatically to the neurons for recognition of the best match in 3 μ S. The full functionality of this IP core is controlled through a set of 3 Read/Write register commands.

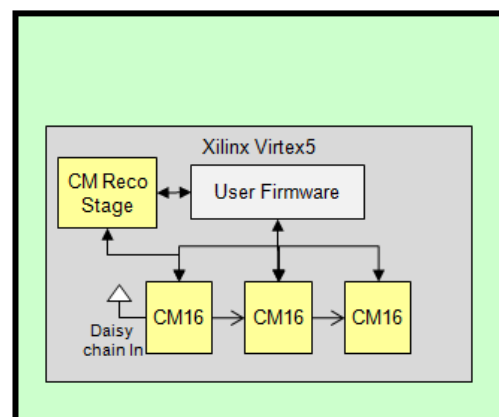
Optional video recognition stage

This IP core allows receiving a video signal through a dedicated input bus, extracting a subsample from a region of interest in the video frame and submitting the resulting vector automatically to the neurons for recognition of the best match in 3 μ S. The full functionality of this IP core is controlled through a set of 6 Read/Write register commands.

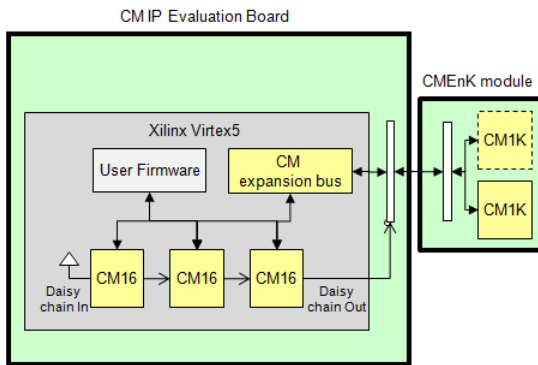
CM IP Evaluation Board



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Optional Inter-chip network expansion



This IP core is necessary to build a network which uses neurons distributed among several chips (identical or not). This IP must be instantiated in each chip holding a portion of the neural network. Testing of this IP core requires that the Evaluation board be equipped with a CMEnK mezzanine board populated with CM1K chips.

Under this configuration, the neurons instantiated in the neuron clusters and the neurons of the CM1K chips become part of a same CogniMem neural network controlled seamlessly by the user firmware through the simple Register Transfer Level operations supported by the neurons.

Evaluation boards

- Choice of FPGA
 - o Xilinx FPGA Virtex 5
 - o Lattice FPGA ESP3
- Choice of communication ports
 - o USB
 - o Ethernet
 - o PCI
- Optional CMEnK mezzanine board with FMC connector

Software

- Test Suites written in Verilog stimulating the different IP cores
- API to access the neurons (on FPGA and silicon) through the CM1K Register Transfer Level protocol

License

- Right to instantiate as many IP core as needed on the Evaluation boards.
- No rights to distribute and instantiate the IP cores on any third party board without prior license from CTI.
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