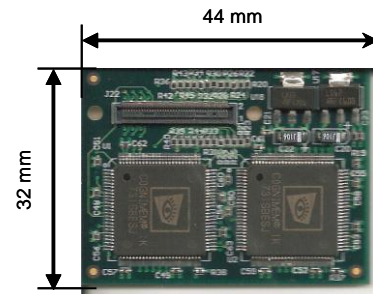


The CME2K is a module populated with two CogniMem chips or 2048 neurons in parallel. Communication is made via a parallel bus or serial bus accessible on the 80-pin Hirose connector. Up to four modules can be stacked on top of each other thus expanding the size of the network by increments of 1024 or 2048 neurons, up to 8192.

### Features

- 1 or 2 CogniMem chips (i.e. 1024 or 2048 neurons)
  - Simple RTL instructions (less than a dozen registers)
  - Parallel bus with data strobe and read/write lines, 5-bit register and 16-bit data lines
  - I2C serial bus (100 and 400 Kbits)
  - Digital input bus for use with the recognition stage built into the chip
- 
- 1 80-pin Hirose connector for single or top-of-stack module
  - Two 80-pin Hirose connectors for in-the-stack modules (symmetrically mounted on each side of the module)

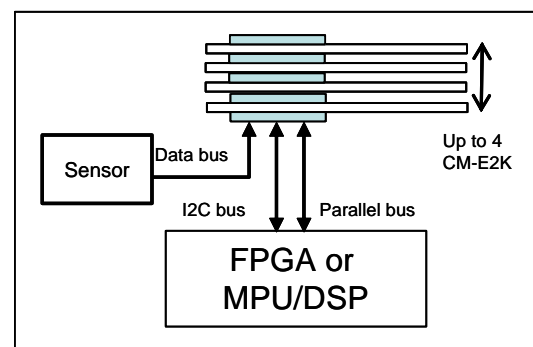


Top side



Bottom side

This module is ideal for prototyping hardware platforms featuring expandable CogniMem neural networks and evaluate their powerful pattern learning and recognition capabilities as well as their speed performance and low power consumption. Typical applications include high-speed vector classification as well as anomaly and event detection. The input source can derive from images, video, signal, sound and more.



Example configuration

The CogniMem™ chip implements two powerful non-linear classifiers (RCE and KNN) in a natively parallel architecture. The tremendous benefit of this architecture is a recognition cycle which remains under 11µs whether the entire network is composed of 1, 2 or more chips. Brute computational power is equivalent to 80 gig operations/second @ 27 MHz for one chip, twice as many for two chips, etc. If the real-time recognition engine built into CogniMem is running, the data received on the digital input bus is automatically broadcasted to the neurons and the response of the neuron with the best match is available in less than 11µs following the last data feed.

### CM1K neural network

- ✓ Parallel architecture with 1024 neurons
- ✓ RCE (Restricted Coulomb Energy)
- ✓ Two classifiers:
  - Radial Basis Function (RBF)
  - K-Nearest Neighbor (KNN) classifier
- ✓ Vector data: up to 256 bytes
- ✓ Classification status: Identified (pin 13), Uncertain (pin 14) or Unknown
- ✓ Categories: up to 32768 values
- ✓ Distance calculation: L1 or LSup distance norms
- ✓ Sub-networks: up to 127 context values
- ✓ Trained by example
- ✓ Recognition stage for direct digital input

### Connectivity

- ✓ Parallel bus
- ✓ Serial bus I2C (100 kbit, 400 kbit and 3.3Mbit)
- ✓ Male and female 80-pin Hirose connectors for stackability
- ✓ Compatible with the CogniMem base boards
- ✓ Up to four stacked modules, totaling 8192 neurons

### Electrical / Mechanical

- ✓ 300 mW @ 27MHz
- ✓ Single source power supply (5 to 12 volts)
- ✓ Average power management w/0.5 watt

### Jumper Configuration

- J20: I2C Enable when jumper is open (trace cut)
- J21: Recognition Enable when jumper is open

### These jumpers apply when recognition is enabled

- J24: Video Enable when open
- J25: Bus Busy propagated enable when shorted
- J26: Category Valid propagated when shorted
- J27: Distance Valid propagated when shorted

### High speed recognition stage for digital input bus

- ✓ V\_clock up to 27 Mhz (pin 15)
- ✓ 8-bit data (pins 18-25)
- ✓ 1 sync. line for vector input (pin 16)
- ✓ 2 sync. lines for video input (pins 16-17)
- ✓ 1 output strobe signal (pin 3) after each vector recognition
- ✓ Digital output bus (pins 4-10)

### Timings

- @ 27 MHz with default vectors of 256 bytes
- ✓ Learning time 10µsec (275 cc)
- ✓ Recognition status in 8µsec (257 cc)
- ✓ Best match in 11µs (275 cc)
- ✓ Subsequent match in 3µs/match (35 cc)

